A 2-Stage Low Noise Amplifier in 90 nm CMOS for 2.4 GHz Applications

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In this paper, a 2-stage low noise amplifier (LNA) is implemented in a 90 nm CMOS technology for 2.4 GHz applications. The measurement results show a noise figure of 3.2 dB with a gain of 19.9 dB. The circuit consumes 6 mA from a 1.2 V supply, and has 7.2 mW power consumption. The core size is 1.1 mm $\times$ 0.95 mm and the chip size including pads is 1.34 mm $\times$ 1.0 mm.

Keywords: 2.4 GHz, LNA, CMOS.

1. INTRODUCTION

With the rapid development and large demand of wireless communication, the low-cost and highly integration has become the essential design targets for the recent communication integrated circuits (ICs). The many new wireless communication standards have been defined that radio-frequency (RF) applications as ZigBee or Bluetooth are taking the market area of short range and low rate communications. Transceiver architecture is shown in Figure 1. Low noise amplifier (LNA) is a core device which directly determines the performance of transceiver system. The first on-chip active stage of a RF front-end is commonly an LNA. Various CMOS LNA topologies have been studied. For example, an energy aware CMOS receiver front end for low power 2.4 GHz application, a wideband low power low noise amplifier in CMOS technology, a low voltage CMOS LNA design utilizing the technique of capacitive feedback matching network, a 2.4 GHz resistive feedback LNA in 0.13 $\mu$m CMOS, a subthreshold low noise amplifier optimized for ultra-low power applications in the ISM band, a modified architecture used for input matching in CMOS low noise amplifiers, a compact 2.4/5.2 GHz CMOS dual-band low noise amplifier, a 2.4 GHz fast switchable LNA with transformer matching for wireless wake-up receivers, a 2.4 GHz single-ended input low power low voltage active front-end for ZigBee applications in 90 nm CMOS, a 2.4 GHz ultra-low power high gain LNA utilizing $\pi$-match and capacitive feedback input network, and a high conversion gain, low noise figure RF CMOS receiver front-end IC for 2.4 GHz applications.

In this paper, a LNA is fully integrated and designed for 2.4 GHz applications in 90 nm CMOS technology. Section 2 explains the LNA design, and Section 3 describes measurement results. The RF receiver designs are explained in Section 4. Finally, Section 5 concludes this work.

2. LNA DESIGN

2.1. Analysis of Matching Circuit

In this circuit, DC voltage is blocked by capacitor which is $C_{in}$ and $C_{ex}$ is used for noise matching and input matching. $L_s$ and $L_g$ are used for input matching, and $L_s$ is degeneration inductor. $L_d$, $C_d$ and $C_{out}$ are used for output matching. Equivalent circuit of small signal analysis for input matching is shown in Figure 3.

We can obtain the following equation for input matching by analyzing the input impedance in Figure 3:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_g} + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s$$  \hspace{1cm} (1)

In order to 50 $\Omega$ termination of input port, real part of input impedance is equal to 50 $\Omega$ and imaginary part of input impedance is equal to zero. Real part of input impedance is $(g_mL_s)/C_{gs}$, and imaginary part of input impedance is $s(L_s + L_g) + 1/sC_g + 1/sC_{gs}$.

2.2. Electromagnetic Simulation

The LNA was designed and fabricated using 1-poly 5-metal 90 nm CMOS technology. This CMOS technology has ultra-thick metal which has thickness of 2.77 $\mu$m, and is located in top metal.
RESEARCH ARTICLE

Fig. 1. Transceiver architecture.

Fig. 2. Schematic of 2-stage LNA.

Fig. 3. Equivalent circuit of small signal analysis for input matching.

Fig. 4. Structure of inductor using EM simulation.

Fig. 5. EM simulated results of inductance and Q factor.

Fig. 6. Microphotograph of the LNA on the PCB.

Fig. 7. Measured and simulated S-parameters.
3. MEASUREMENT RESULTS

The LNA circuit was fabricated using 90 nm CMOS technology. A microphotograph of the LNA on the PCB is shown in Figure 6. The figure is shown that the LNA circuit was characterized by on-PCB measurements using SMA connector, and the figure shows 2-port measurement setup for measurements of S-parameters and noise figure. Figure 7 shows measured and simulated S-parameters. S-parameter measurements were carried out using RF cable, 2.9 mm to SMA adaptor and Agilent E8358A network analyzer. The measurement result of input return loss is 24.6 dB at 2.4 GHz, and the output return loss is 5.6 dB at 2.4 GHz. S21 is gain in LNA and 19.9 dB at 2.4 GHz.

As inductor has more thickness, inductor has higher quality factor. Therefore, the top metal has ultra-thickness in RF systems.

Figure 4 depicts structure of inductor using electromagnetic (EM) simulation. This inductor has width of 6 μm and 6.5 turn.

Figure 5 shows EM simulation results of inductor specification such as inductance and Q factor. This inductor has inductance of 7.7 nH at 2.4 GHz and Q factor of 6 at 2.4 GHz. We obtain optimized inductors and interconnection lines using EM simulation.

### Table I. Comparison of simulation and measurement results.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation</th>
<th>Measurement</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>90 nm CMOS</td>
<td></td>
</tr>
<tr>
<td>S11 (@2.4 GHz) [dB]</td>
<td>-22.3</td>
<td>-24.6</td>
</tr>
<tr>
<td>S22 (@2.4 GHz) [dB]</td>
<td>-10.3</td>
<td>-5.6</td>
</tr>
<tr>
<td>S21 (@2.4 GHz) [dB]</td>
<td>20.5</td>
<td>19.9</td>
</tr>
<tr>
<td>Noise figure (@2.4 GHz) [dB]</td>
<td>2.7</td>
<td>3.2</td>
</tr>
<tr>
<td>Input P1dB [dBm]</td>
<td>-21.6</td>
<td>-21</td>
</tr>
<tr>
<td>Power consumption [mW]</td>
<td>7.99</td>
<td>7.2</td>
</tr>
<tr>
<td>Chip size* [mm²]</td>
<td>1.34 x 1</td>
<td></td>
</tr>
</tbody>
</table>

Note: *Including pad.
Measurement and simulation results of noise figure are shown in Figure 8. Noise figure measurement was measured using Agilent N8975A noise figure analyzer. The measurement result of noise figure is 3.2 dB at 2.4 GHz. The power consumption of LNA is 7.2 mW, and input P1dB is ~21 dBm. The effective area of the LNA is 1.1 × 0.95 mm² and including pad size is 1.34 × 1 mm². Comparison of simulation and measurement results at 2.4 GHz are shown in Table I. These table and figures show that measured results is similar to simulated results. Using EM simulation of accurate structure, we obtained these results.

### 4. RECEIVER DESIGN

Key components of receiver are LNA and mixer. Mixer has a variety of topologies. The mixer is designed using single balanced active structure. Active mixer has power consumption. However, active mixer can obtain conversion gain. Figure 9 shows a schematic of single balanced active mixer.

The simulated result of input return loss is 15.4 dB at 2.4 GHz and conversion gain is 15.8 dB at 10 MHz. The power consumption of mixer is 4.75 mW. Figure 10 depicts layout of the single balanced active mixer. This figure shows that LO input is differential signal and symmetric structure.

The effective area of mixer is 1.26 × 0.72 mm² and including pad size is 1.5 × 0.82 mm². The layout of receiver is shown in Figure 11. The receiver structure consists of LNA and active mixer. The simulated result of input return loss is 17 dB at 2.4 GHz and conversion gain is 44.2 dB at input power of −40 dBm. The power consumption of receiver is 12.74 mW. The effective area of receiver is 2.37 × 0.95 mm² and including pad size is 2.61 × 1 mm². Summarization of simulated results about active mixer and receiver at RF frequency of 2.4 GHz and IF frequency of 10 MHz are shown in Table II.

### 5. CONCLUSIONS

This letter presented a 2.4 GHz 2-stage LNA in 90 nm CMOS technology. The amplifier has gain of 19.9 dB and consumes DC power of 7.2 mW. Then, the mixer and receiver were designed based on the LNA using 90 nm CMOS technology. The receiver results show that conversion gain of 44.2 dB and noise figure of 4.23 dB.

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### References and Notes


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