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Low-power CMOS Front-end ROIC using Inverter-feedback RGC TIA for 3-D Flash LADAR Sensor

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Abstract—**This work proposes a pixel architecture for a front-end readout integrated circuit (ROIC) using an inverter-feedback regulated-cascode (RGC) trans-impedance amplifier (TIA) for the focal plane array of a three-dimensional flash laser detection and ranging sensor. Although there are various TIA topologies for wideband operation, the inverter-feedback RGC structure is adopted owing to the importance of the small area and low power consumption of the array configuration. A single pixel also consists of an overcurrent protector, comparator, amplitude-to-voltage converter, and time-to-voltage converter to sense the range and intensity information of the remote object. A single pixel dissipates a power of 5.28 mW from a 3-V supply. The receiver achieves an input referred noise current of 7.5 pA/√Hz with a bandwidth of 453 MHz, transimpedance gain of 76 dB·Ω, and a maximum detection range of 60 m with a 3.8-ns pulse. A single pixel is developed within 100 μm × 100 μm and the total die size, including the I/O pads, is 2200 μm × 2200 μm.**

Index Terms—**Laser detection and ranging (LADAR) sensor, readout IC (ROIC) array, optical receiver, flash LADAR, focal plane array**

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I. INTRODUCTION

A laser detection and ranging (LADAR) sensor is an active imaging sensor that can acquire real-time three-dimensional (3-D) imagery of targets by emitting and detecting laser pulses. It has been deployed in many applications such as reconnaissance, autonomous vehicles and robots, remote sensing, and surface mapping for buildings and scenes where high 3-D resolution is of prime importance [1-5]. For high-precision 3-D image acquisition, a pulsed time-of-flight (TOF) LADAR sensor is widely used to measure distances, compared with other measurement methods such as the continuous-wave optical phase method [6, 7] or structured light-based method [8]. Generally, a pulsed LADAR sensor consists of a laser transmitter, optical receiver, and signal processor module, as shown in Fig. 1. The outgoing laser pulse passes through the transmission optics, reflected from a target, and focused onto the photodetector through the receiver lens. The time between the launching of the pulse and its return is proportional to the range via the velocity of light. The receiver converts the detected optical signal into an electrical current pulse using a photodetector, converts the current into a voltage using a transimpedance amplifier (TIA), detects the pulse amplitude using an amplitude detector, produces a timed logic pulse (STOP) that indicates the arrival of the return signal using a comparator, and converts the TOF into a voltage using a timing detector.

There are various operation methods for the pulsed LADAR sensor with different scanning mechanisms,

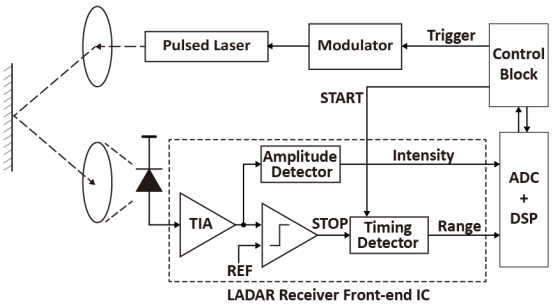

Fig. 1. Block diagram of the typical pulsed LADAR sensor.

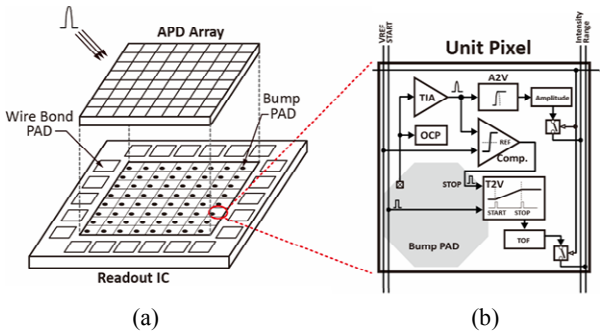

Fig. 2. Block diagram of the proposed transmitter.

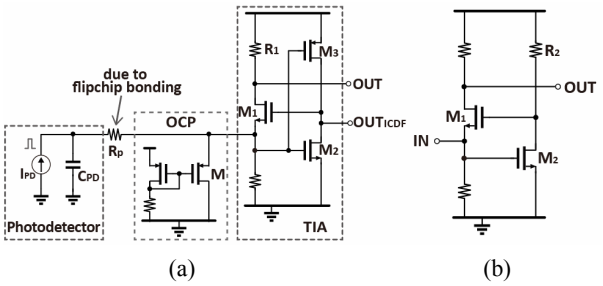

Fig. 3. Schematic of (a) implemented inverter-feedback RGC TIA with an OCP and photodetector model, (b) conventional RGC-TIA.

number of lasers, and geometric configurations [9-11]. In particular, a 3-D flash LADAR sensor can detect the 3-D image of an object moving very fast by measuring the TOF of the pulsed laser. A 3-D flash LADAR sensor obtains an entire frame of 3-D data by using a single-short laser pulse and a focal plane array (FPA) of photodetectors, along with its corresponding front-end readout integrated circuits (ROICs) [11]. There are many challenges in designing the ROIC. Especially, in an array configuration, extensive power management would be necessary to keep the power consumption to a reasonable level [12]. Additionally, the size of the circuits for the ROIC should be small enough to fit within the pixel dimension.

This paper focuses on the TIA for a low-power pixel implementation for the FPA. Among the various TIA topologies available for wideband operation, a pixel architecture using the inverter-feedback regulated-cascode (RGC) structure is proposed, owing to its low power consumption and small-area characteristics. The implemented ROIC consists of an overcurrent protection circuit (OCP), comparator, amplitude-to-voltage converter (A2V), and time-to-voltage converter (T2V). The ROIC for a unit pixel and its array are implemented in 0.18-μm CMOS technology for a flash LADAR sensor using avalanche photodiode (APD) detectors. The proposed pixel is developed within 100 μm × 100 μm for high resolution, and this pixel is expanded to a 2 × 8 array. The amount of current consumed by a proposed unit pixel is approximately 1.76 mA.

II. Proposed Pixel Architecture

Fig. 2(a) is an illustration of the simplified 3-D FPA [11].

Each photodetector is connected to its corresponding ROIC via a metal bump. The proposed pixel architecture is illustrated in Fig. 2(b). The unit pixel consists of five parts: TIA, OCP, comparator, A2V, and T2V. They should not consume much power in an array configuration, and the size of these components should be small enough to fit the pixel dimension.

First, the TIA, as a low-impedance input stage, amplifies the received photocurrent from a photodetector. The proposed pixel adopts an inverter-feedback RGC TIA, as shown in Fig. 3(a), rather than an inverter-type [13], shunt-feedback topology [14], C-TIA topology [15], or conventional RGC TIA [16]. Although the RCG structure has a slightly higher input-referred current noise than that in others, all other topologies, except the RGC structure, consume a large amount of current or occupy a large area. Hence, they are not considered. This work compares three different TIA structures intended for use in the pixel for a flash LADAR sensor. They are the inverter-feedback RGC TIA, an inverter based common-drain active feedback (ICDF) TIA [17], and conventional RGC TIA. The difference between the inverter-feedback TIA and ICDF TIA is the output node and the main amplifier or feedback stage. The inverter-feedback RGC output is taken from the drain of the common-gate

amplifier, as shown in Fig. 3(a), just as in the conventional RGC TIA, as shown in Fig. 3(b). The ICDF TIA output node is OUT_{ICDF}, which is the drain of the inverter amplifier in Fig. 3(a). The transimpedance gain of the inverter-feedback RGC TIA is the same as that of the conventional RGC-TIA and is given by:

$$Z_{T,INV-RGC} \cong R_1 . \tag{1}$$

The transimpedance gain of the ICDF structure, where resistor R_1 is replaced by a PMOS transistor M_3, is given by:

$$\begin{aligned} Z_{T,ICDF} &\cong \frac{\left(r_{ds1}+R_1\right)\cdot A_{INV}}{1+g_{m1}r_{ds1}\left(1+A_{INV}\right)} \\ &\cong \frac{1+R_1/r_{ds1}}{g_{m1}} \qquad if\ A_{INV} \gg 1, \end{aligned} \tag{2}$$

where g_{m1} and r_{ds1} are the transconductance and output resistance of M_1, respectively, and A_{INV} is the voltage gain of the inverter stage. The transimpedance gain is determined by the ratio of $1+R_1/r_{ds1}$ and g_{m1}.

The TIA bandwidth is limited by the parasitic parallel capacitance $\left(C_{PD}\right)$ owing to the large area of the photodetector and the parasitic series resistance (R_P) owing to flip-chip bonding, shown in Fig. 3(a). The small-signal input impedance of the inverter-feedback or ICDF structure is approximately given by (3)

$$\begin{aligned} Z_{in,INV-RGC} &\cong \frac{1}{g_{m1}\left(1+A_{INV}\right)} \\ &= \frac{1}{g_{m1}\left(1+\left(g_{m2}+g_{m3}\right)\left(r_{ds2}//r_{ds3}\right)\right)}, \end{aligned} \tag{3}$$

where g_{m1}, g_{m2}, and g_{m3} are the transconductances of M_1, M_2, and M_3, respectively.

The small-signal input impedance of the conventional RGC TIA, as shown in Fig. 3 (b), can be calculated from (4).

$$\begin{aligned} Z_{in,RGC} &\cong \frac{1}{g_{m1}\left(1+A_{CS}\right)} \\ &= \frac{1}{g_{m1}\left(1+g_{m2}\left(R_2//r_{ds2}\right)\right)}, \end{aligned} \tag{4}$$

Table 1. TIA Performance Comparison

	This work	ICDF-RGC	Conventional-RGC
C_{PD} [pF]	1	1	1
Transimpedance gain [dBΩ]	76	61	76
Bandwidth [MHz]	453	456	420
Input-referred noise [pA/√Hz]	7.5	12.3	7.7
Current consumption [mW]	0.27	0.27	0.21
Size of M_3 or R_2 (L/W)	1.9 μm × 8 μm (7.2 μm^2)	0.9 μm × 8 μm (7.2 μm^2)	8 μm × 1.4 μm (11.2 μm^2)

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. The input impedance of the inverter-feedback RGC TIA or ICDF TIA can be lower than that of the conventional RGC structure owing to the large voltage gain of the inverter stage.

The three TIA topologies are designed and simulated for performance comparison. Except the resistor R_2 in Fig. 3(b), all other component values for the conventional RGC TIA are the same as those of the inverter-feedback TIA in Fig. 3(a). The simulation results are summarized in Table 1. The ICDF TIA has lower transimpedance gain and higher input-referred noise current than other topologies. The inverter-feedback RGC TIA and the conventional RGC TIA show similar simulation results. However, the size of R_2 in the conventional RGC TIA is approximately 1.5 times larger than the size of M_3 in the inverter-feedback RGC TIA. Moreover, in many CMOS technologies, the process variation of the resistor is larger than that in a MOS transistor. In order to minimize the inter-pixel variation in the array structure, the inverter-feedback RGC TIA using a MOS transistor instead of a resistor is selected.

The bandwidth required for the TIA to preserve its rise time, can be approximated from [6] as

$$BW \cong \frac{0.35}{t_r}, \tag{5}$$

where t_r is the rise time of the input pulse. In this work, the full width at half maximum (FWHM) of the input pulse is approximately 3.8 ns and its rise time is approximately 1 ns. For a rise time of 1 ns, (5) gives a bandwidth of approximately 350 MHz. With a photodetector parasitic parallel capacitance C_{PD} of 1 pF

and parasitic series resistance R_p at 100 Ω, the simulated bandwidth of the designed TIA is approximately 453 MHz. The TIA achieves an input referred noise current of 7.5 pA/√Hz with a bandwidth of 453 MHz and a transimpedance gain of 76 dB·Ω. The amount of current consumed by the TIA is approximately 0.27 mA per pixel.

The OCP, as shown in Fig. 3, is designed to protect the pixel from being damaged by the very high input photocurrent. [13]. Transistor M only turns on when its source voltage is greater than 1.7 V, and size of the transistor M is big enough to sink several milliamperes. When the input current is approximately 200 μA, the source voltage of M reaches 1.7 V.

The remaining circuits in the pixel are conventional circuits that occupy a small area. The simplest way of defining the timing point is the leading-edge technique, in which the rising edge of the signal is compared with the constant threshold voltage [6]. A comparator produces a STOP signal, which is a timed logic pulse that indicates the arrival of the return signal. The comparator implemented in the pixel consists of a decision stage [18] and post-amplifier [19]. A2V detects the amplitude of the return pulse using a peak-detect-and-hold circuit (PDH) and sample-and-hold circuit (SH). The PDH used in this pixel was proposed by Kruiskamp and Leenaerts in 1994 [20, 21]. The SH is designed to be turned on for a short time at the falling edge of the comparator output pulse to save the intensity information. Finally, T2V proportionally converts the time between START and STOP into a voltage [22]. The implemented T2V is able to measure time intervals over a linear range of 30 – 400 ns, which corresponds to 60 m.

A functional diagram of the fabricated chip is shown in Fig. 4. The designed ROIC of 2 × 8 pixels is placed in an 8 × 8 pixel array. To read the stored intensity and range information in each pixel, an eight-channel decoder for row selection; a 16-to-1 multiplexer for column and output type, intensity, and range; and an output buffer of 50 Ω for output impedance matching are additionally designed.

To characterize the designed ROIC array without a flip-chip bonded photodetector, it is impossible to induce the current pulse in every pixel via I/O pads. In this work, a switch is added to each input path, and all inputs of the switch are connected to a single node, as shown in Fig. 5.

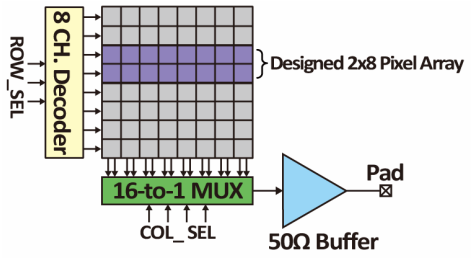

Fig. 4. Functional diagram of fabricated chip.

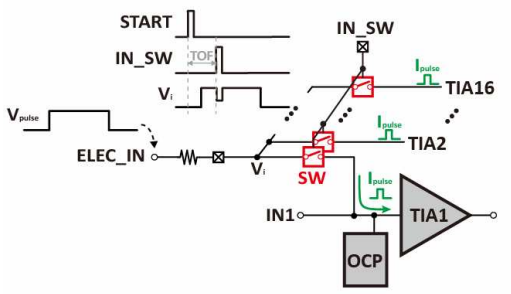

Fig. 5. Operation principle of input path switch for array test with electrical current pulse.

A long voltage pulse is applied to ELEC_IN. Once IN_SW is shortly turned on, the current pulse with the same pulse width as IN_SW is passed through the switch. This electrical current pulse is concurrently induced in every pixel with the same amplitude.

III. Measurement Results

The designed ROIC of 2 × 8 pixels was fabricated using a standard 0.18-μm CMOS process a micro-photograph of the fabricated chip is shown in Fig. 6. The total chip size, including the I/O pads, is 2200 μm × 2200 μm, and the unit pixel occupies an area of 100 μm × 100 μm. All DC biases were connected to an external power supply through bonding wires.

An example of the waveform of key signals involved in the designed pixel array is illustrated in Fig. 7. All signals are generated from an external control board with an FPGA. A global clock signal CLK modulated at a frequency of 40 MHz is used as a reference signal. The EN signal can be used as a trigger signal for the laser transmitter and measurement equipment. When EN is high, the pixel receives the input signal and stores the pulse intensity and range. In the discriminate-and- hold mode, the START and IN_SW signals are enabled for a clock at intervals of TOF. The read operation starts when

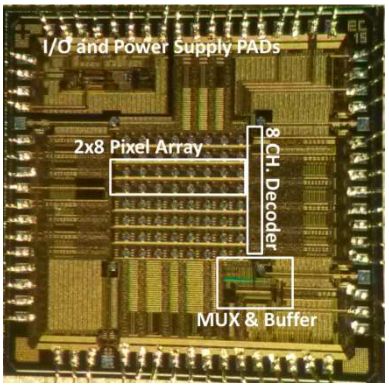

Fig. 6. Functional diagram of fabricated chip.

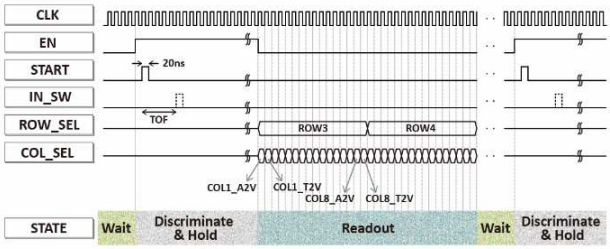

Fig. 7. Sensor timing diagram.

EN is low. In the readout operation, the selection of 32 outputs can be accomplished with ROW_SEL for row selection and COL_SEL for a 16:1 data mux, which is for the readout of stored data in each pixel through an output pad. For each pixel, the peak amplitude from A2V and the range information from T2V are selected by turns.

To facilitate the measurement of the electrical pulse response, the fabricated chip was mounted on an FR-4 PCB test fixture. The measurement setup is described in Fig. 8. A long electrical pulse, generated from a function generator, was applied to ELEC_IN of the implemented test fixture. The OUT signal was measured by using an Agilent DSO7104B oscilloscope. To control the operation of the fabricated array circuit, an external control board with an FPGA was implemented. It generates EN, START, IN_SW, ROW_SEL, and COL_SEL from a global clock signal CLK.

Fig. 9 shows the measured A2V and T2V outputs corresponding to an input current of 26, 31, and 36 μA with a TOF of 100 ns. The A2V output increases with the input current, but the T2V output is the value for a TOF of 100 ns. By contrast, Fig. 10 shows the measured output voltages corresponding to a TOF of 60, 80, 100, and 200 ns with an input current of 26 μA. The T2V output increases with the TOF but the A2V output

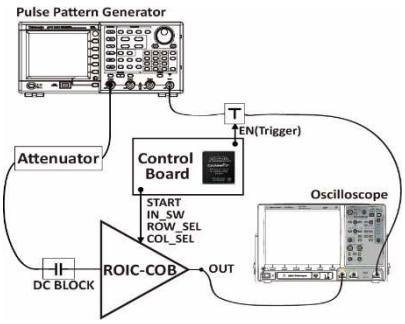

Fig. 8. Measurement setup for electrical pulse test.

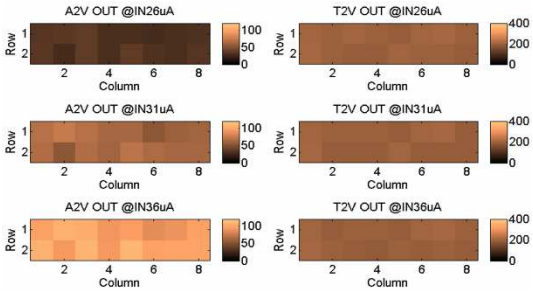

Fig. 9. Measured intensity and range map vs. input current amplitude.

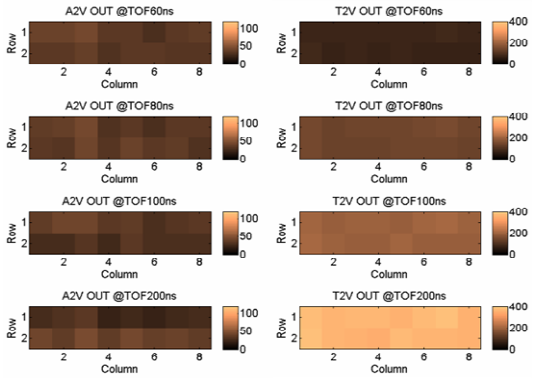

Fig. 10. Measured intensity and range map vs. TOF.

maintains the level for an input current of 26 μA. From these results, the designed array ROIC is able to generate 3-D images according to the intensity and TOF of the return pulse, and it has the potential to be scaled to a larger FPA using the designed pixel.

A single pixel dissipates a power of 5.28 mW. The total power consumption for 2 × 8 pixels, including 54 mW of the output buffer for 50-Ω impedance matching, is 138.5 mW from a 3-V supply.

Table 2 gives a performance summary of the proposed LADAR sensor in comparison with recently published works. It is clear from the table that a significant improvement is achieved in the power consumption, with

Table 2. Receiver Performance Comparison

	This work	[5]	[13]	[15]
Array	2 × 8	1	1	1
C_{PD} [pF]	1	1.5	2	2.5−5
Transimpedance gain [dBΩ]	76	81	78	80
Bandwidth [MHz]	453	230	640	160
Input-referred rms noise [μA]	0.16	0.05	0.12	0.02
Power consumption [mW]	5.28*	115	114	79
Chip size [mm^2]	2.2 × 2.2	1.85 × 1.85	0.89 × 0.66	1.2 × 1.2
Technology	CMOS 0.18 μm	BiCMOS 0.35 μm	CMOS 0.13 μm	CMOS 0.35 μm

an acceptable bandwidth of 453 MHz.

V. CONCLUSIONS

An integrated, wideband, and low-power ROIC for unit pixels, intended for use in a 3-D flash LADAR sensor, and its 2 × 8 array were designed, implemented, and tested with an electrical current pulse in the present work. The measurement results confirmed that the operation of the array ROIC is in accordance with the working principle of the FPA for a flash LADAR sensor.

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